IBM Research

Reliability of advanced CMOS devices and circuits

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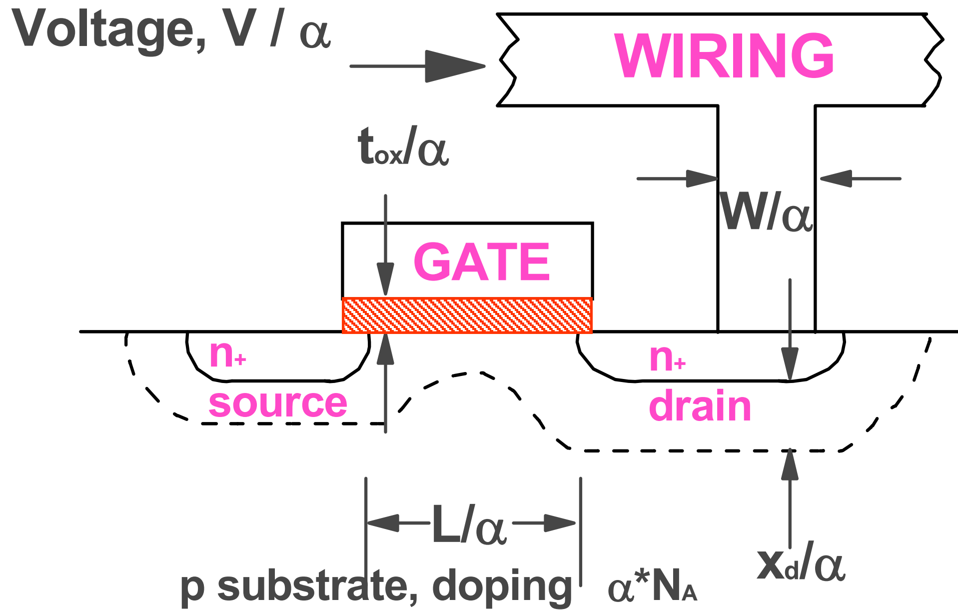
CMOS Scaling Rules



SCALING:

Voltage: V/α

Oxide: t_{ox}/α

Wire width: W/α

Gate width: L/α

Diffusion: x_d/α

Substrate: αN_A

R. H. Dennard *et al.*,
IEEE J. Solid State Circuits, (1974).

RESULTS:

Higher Density: $\sim\alpha^2$

Higher Speed: $\sim\alpha$

Power/ckt: $\sim 1/\alpha^2$

Power Density: ~Constant

t_{ox} scaling required for short channel control

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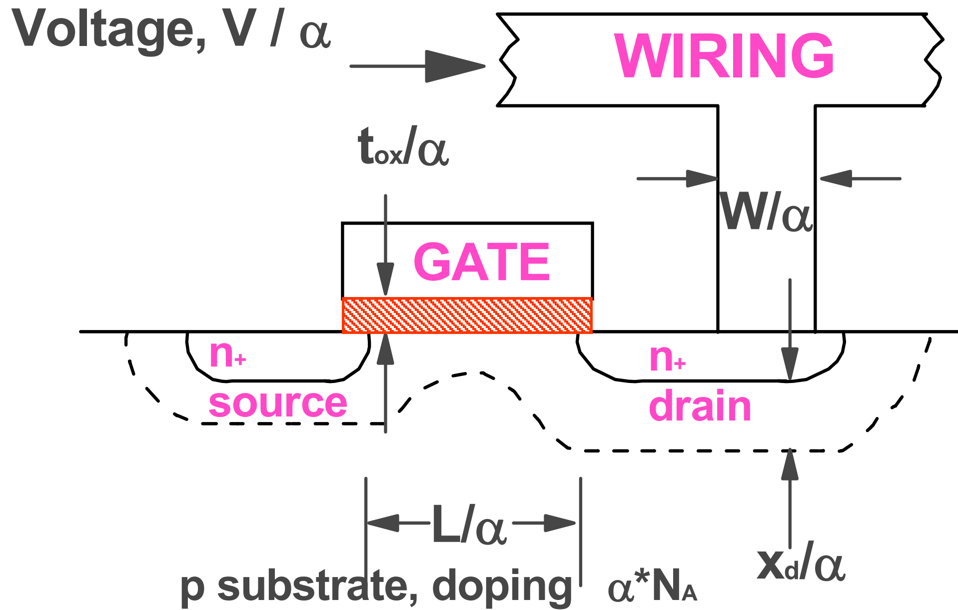
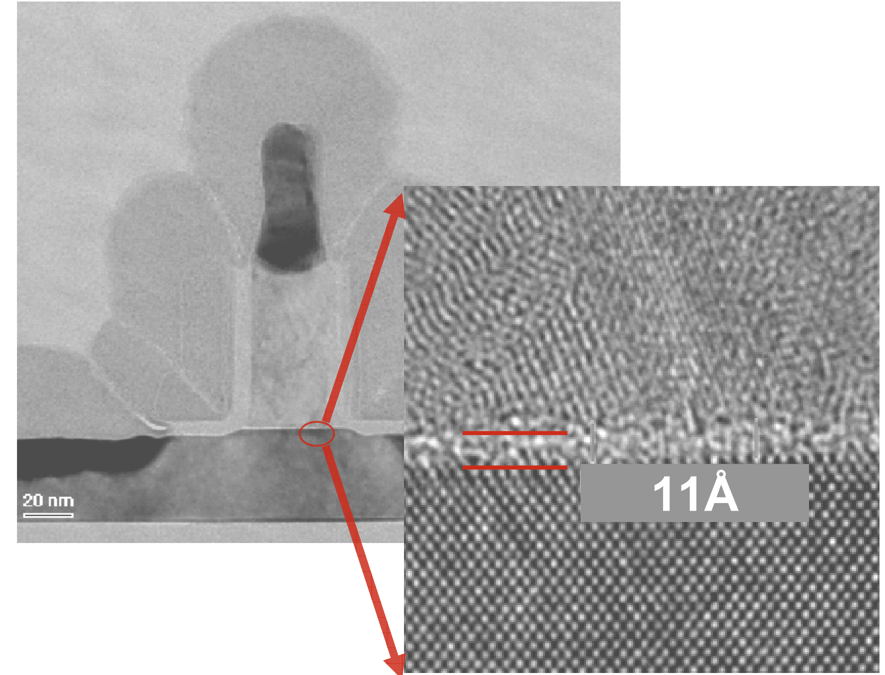
CMOS Scaling Rules





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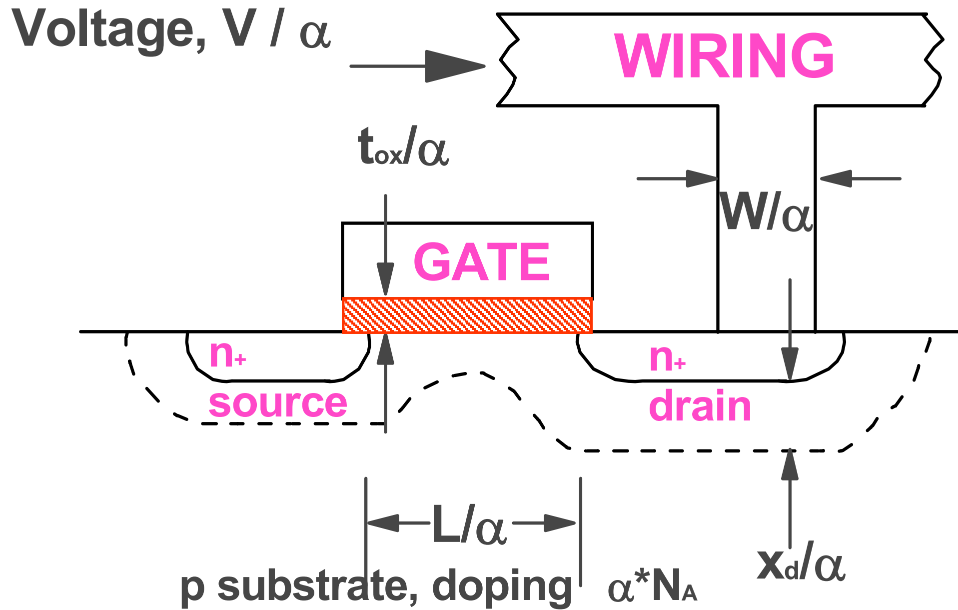

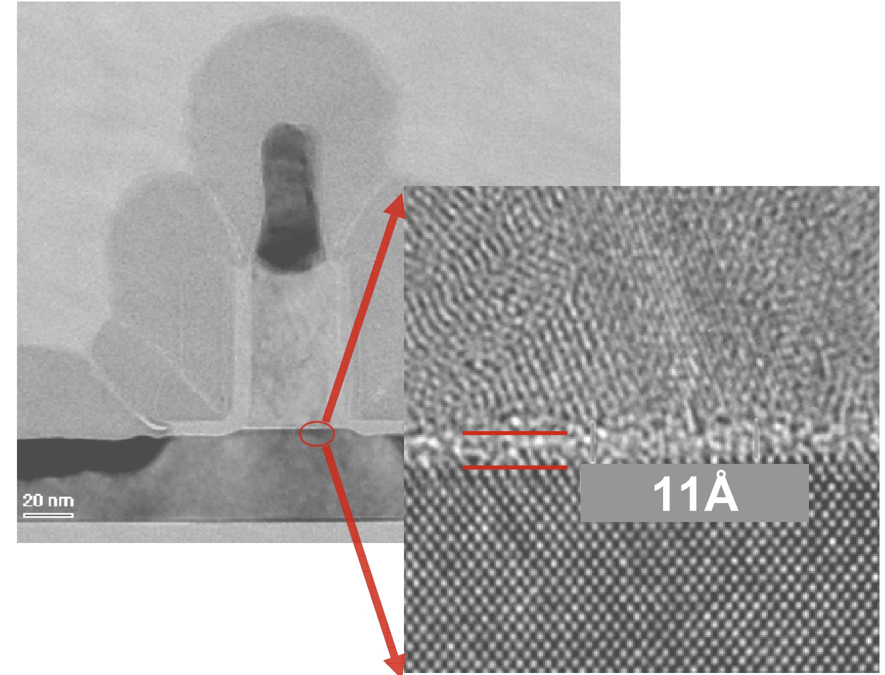

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t_{ox} scaling required for short channel control

- Approaching atomistic and quantum-mechanical boundaries
- **Atoms are not scalable!**

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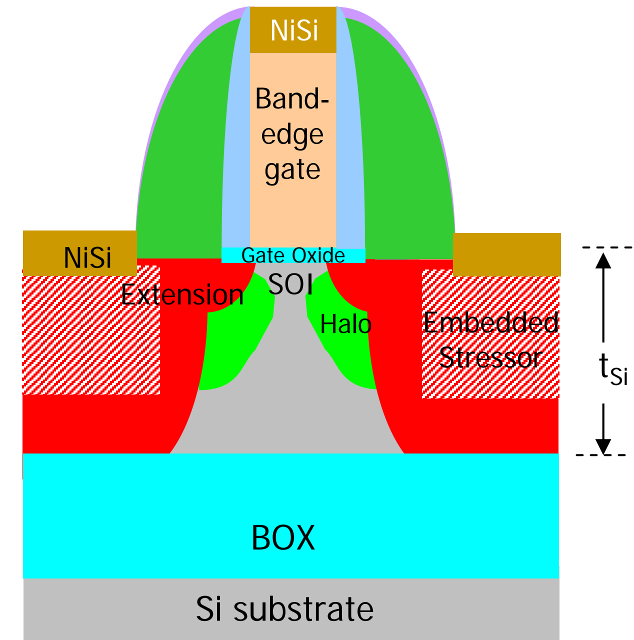
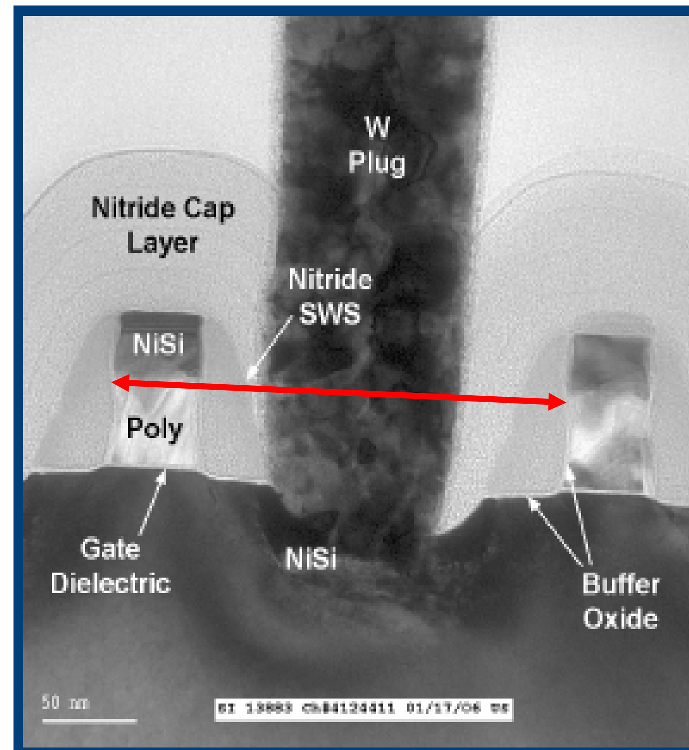
Device Scaling

- **Conventional bulk device or partially-depleted SOI (PDSOI)**
  - Aggressive gate dielectric scaling for improved short channel control
  - Increased random doping fluctuations due to width and length scaling
  - Spacer thickness decreasing
    - Becoming comparable to old gate dielectric thickness (~10nm)





Node	Device Pitch (nm)
45	170-180
32	120-130
22	80-100
15	65-80
11	50-65

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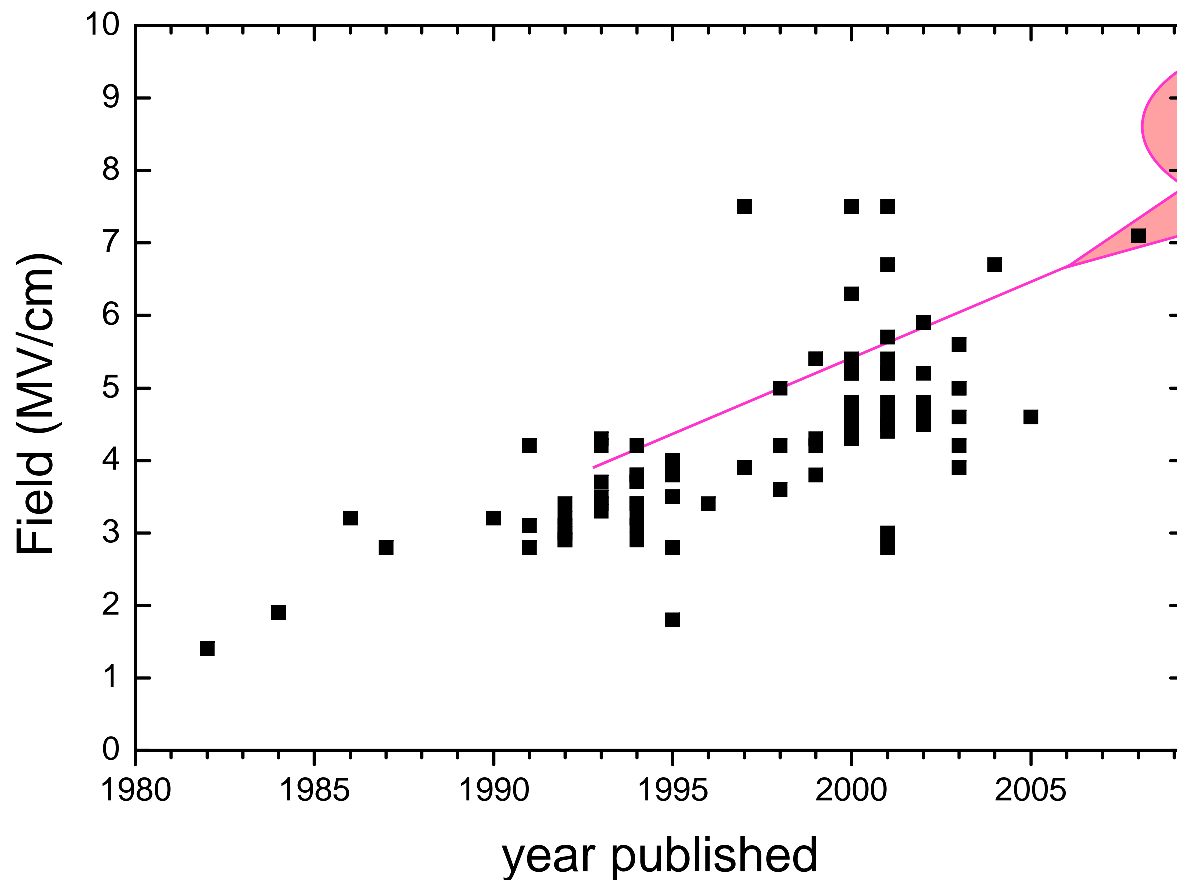
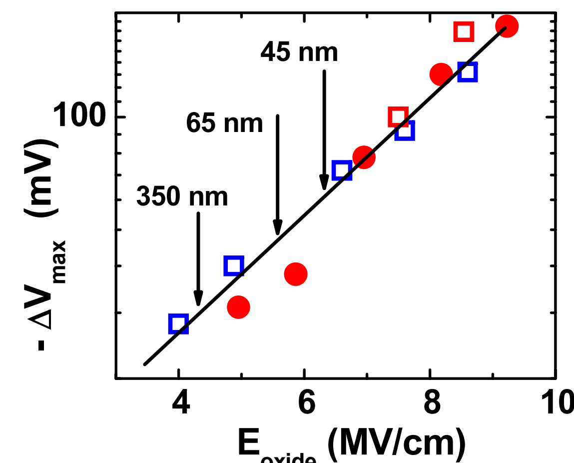
CMOS Scaling:
Oxide electric field increasing





- estimated NBTI at 10 years

source: IEDM and VLSI

$$E_{ox} = (V_{gate} / t_{electrical}) = (CV/\varepsilon)$$

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Major MOSFET oxide failure mechanisms

- **Bias/Temperature Instability**
  - NBTI
  - PBTI
- **Dielectric Breakdown**

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Negative-bias-temperature instability

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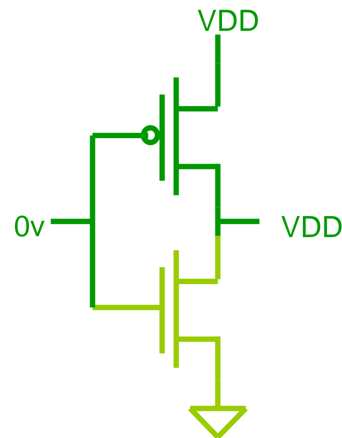
Negative-bias-temperature instability

pFET on-state



Bias conditions during circuit operation of a CMOS inverter. With input at Ground, output is High and the p-MOS device (top) is under uniform negative gate bias with respect to its substrate.

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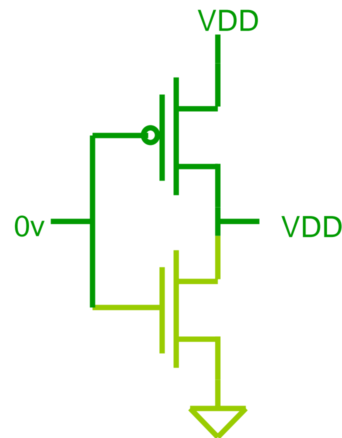
Negative-bias-temperature instability

pFET on-state

Thermal activation (~0.2eV)



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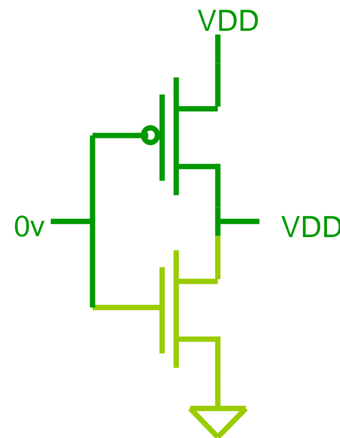

Bias conditions during circuit operation of a CMOS inverter. With input at Ground, output is High and the p-MOS device (top) is under uniform negative gate bias with respect to its substrate.

- **Believed to be caused by an electrochemical reaction with a hydrogen related species in the oxide, reacting with holes in the pfet channel.**
- **First described by Miura and Matukura. Jpn. J. Appl. Phys., vol. 5, p. 180, *1966*.**

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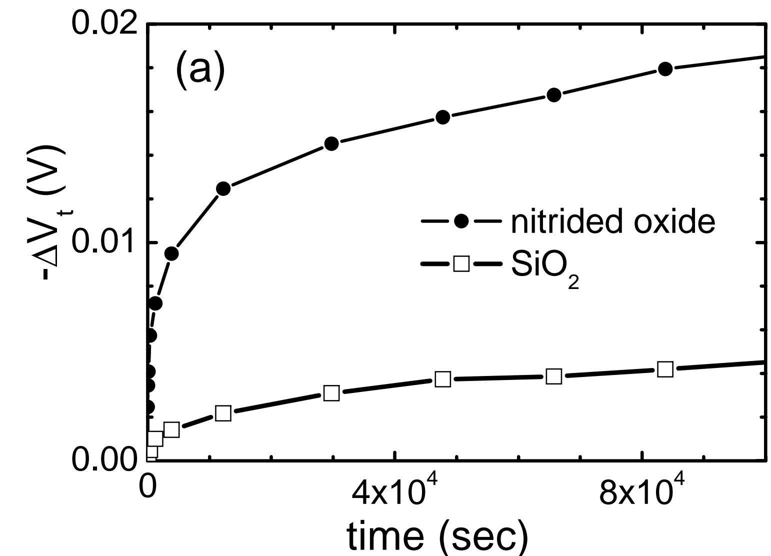
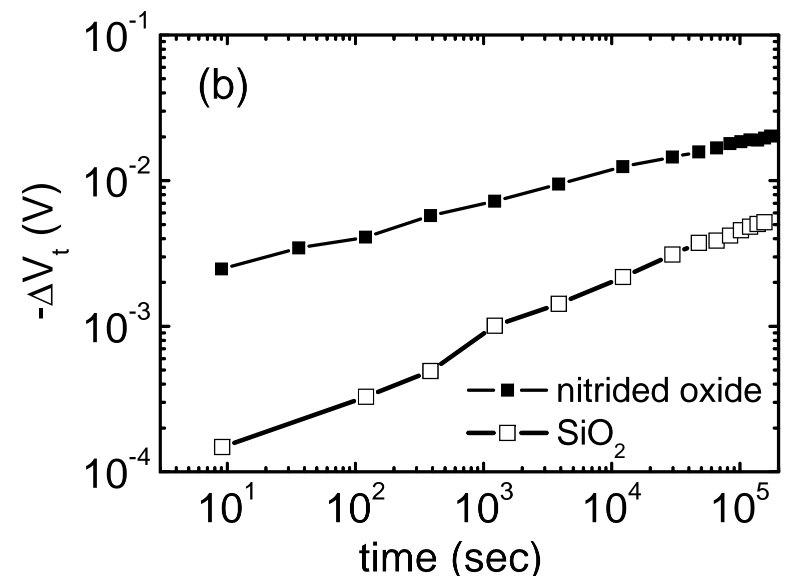
Negative-bias-temperature instability (NBTI)

- **Basic features:**
  - **PFET** threshold voltage shift
    - negative threshold voltage (V_t) shift
    - interface states and positive oxide charge
    - → drive current reduction
    - → circuit speed reduction
  - Power law time dependence
  - Nitrided oxide has larger shift and shallower slope
    - Nitridation of gate oxide makes it worse





- "The Negative Bias Temperature Instability in MOS Devices: A Review", J.H. Stathis and S. Zafar, Microelectronics Reliability, **46**, 270-286 (2006).

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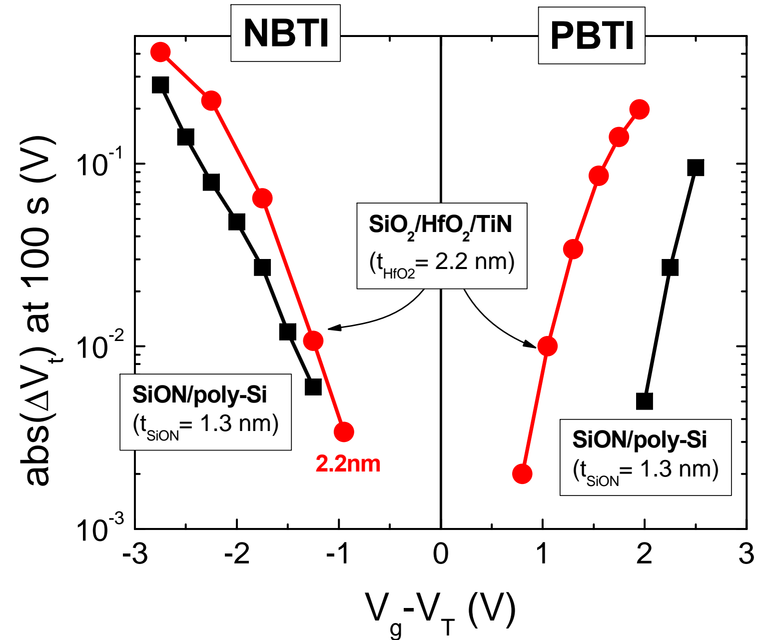
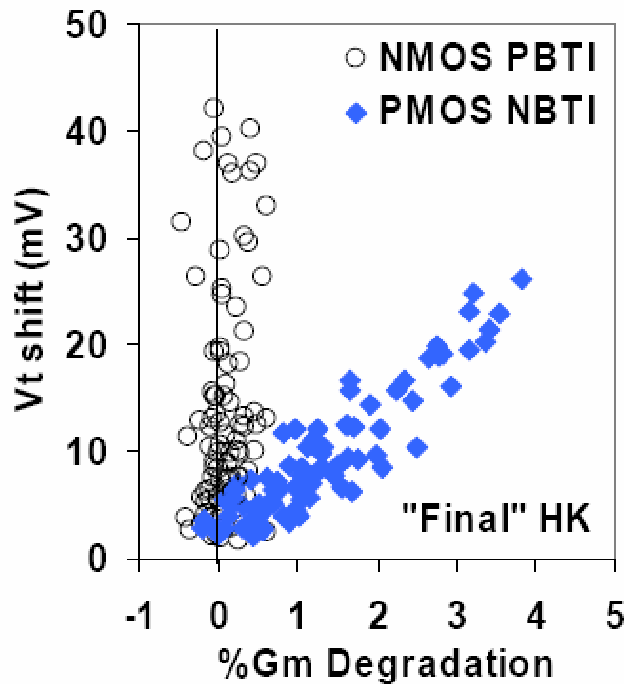
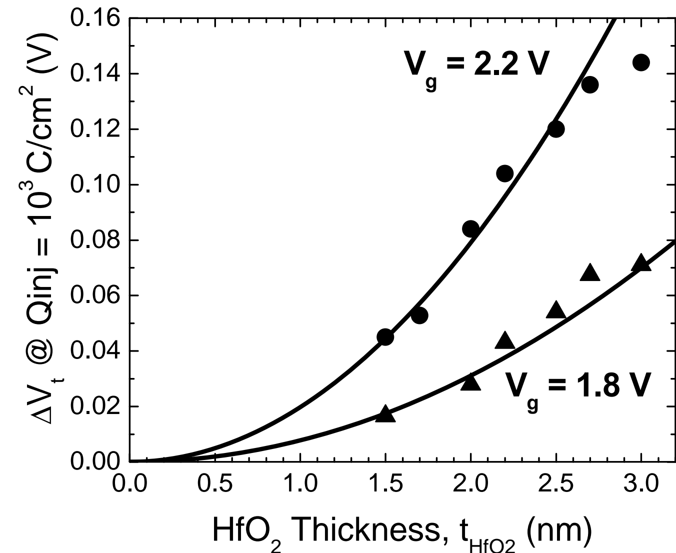
"PBTI" in high-k NFET

- **"PBTI" is a V_t shift observed under positive bias (*i.e.,* in n-FET)**
  - Not seen in SiO_2/poly under normal use conditions
  - Charge trapping in high-k layer





- S. Pae *et al.*, IRPS 2008.



- A. Kerber *et al.*, to be published, IEEE Trans. Dev. and Mater. Reliab.

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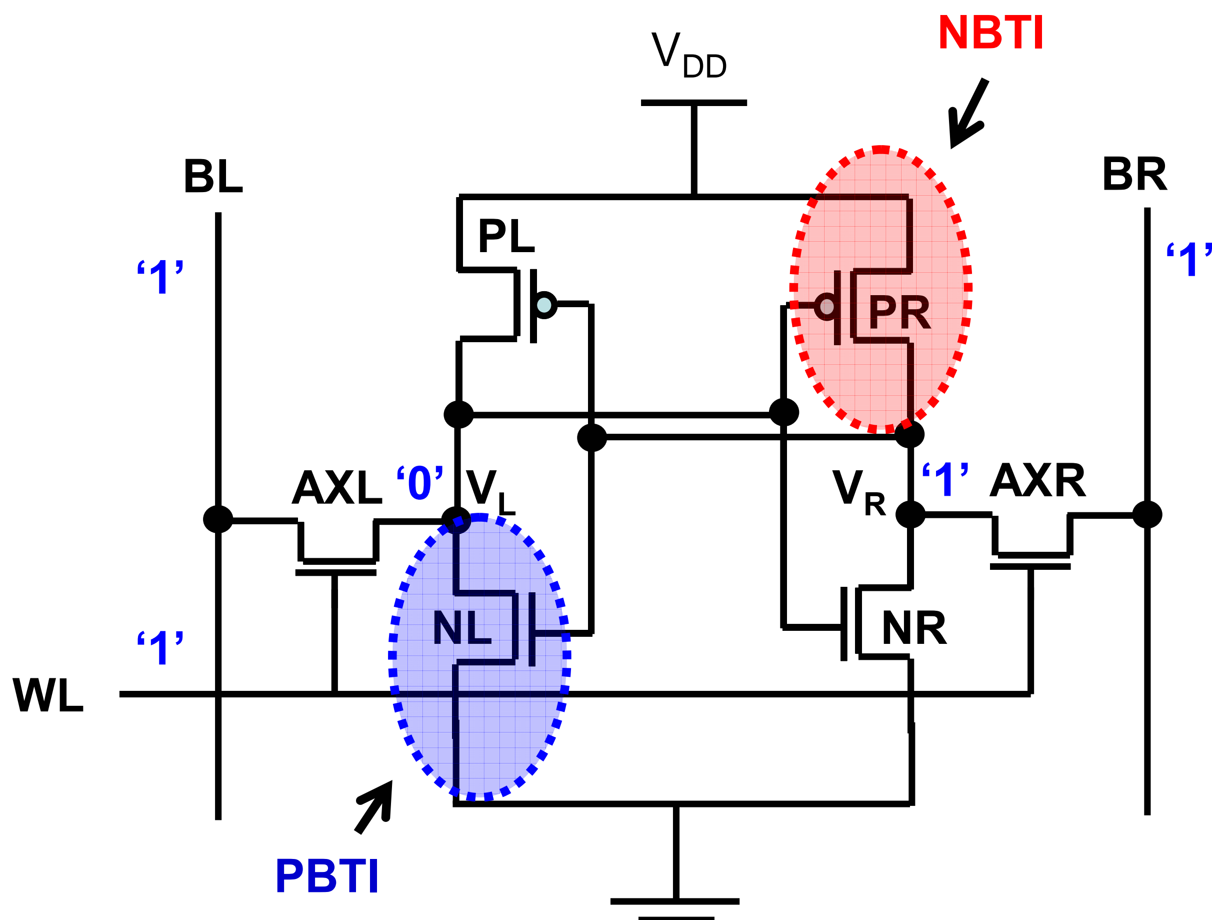
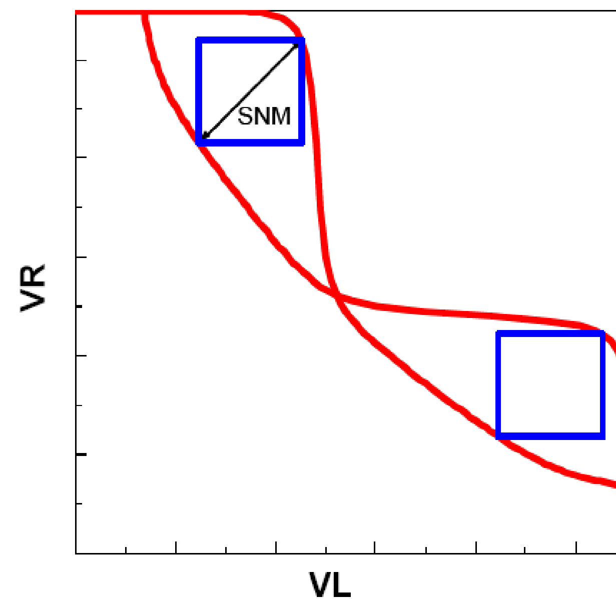
NBTI and PBTI in SRAM



- **Static noise margin analysis (butterfly curve)**



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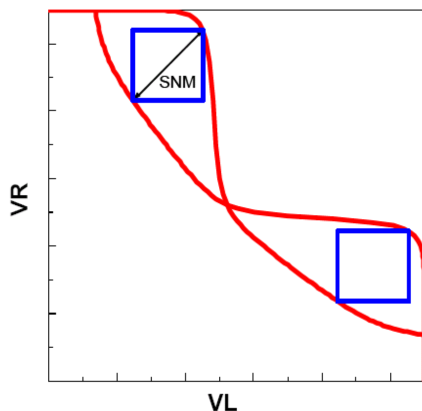
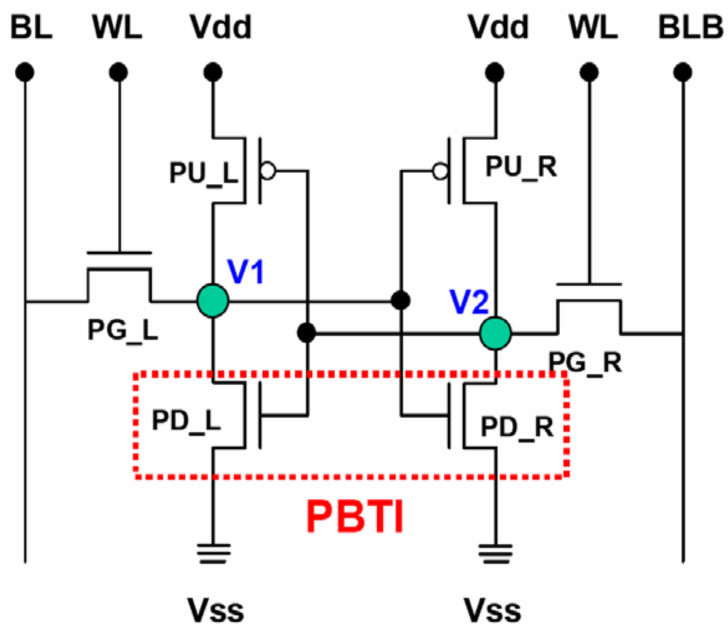
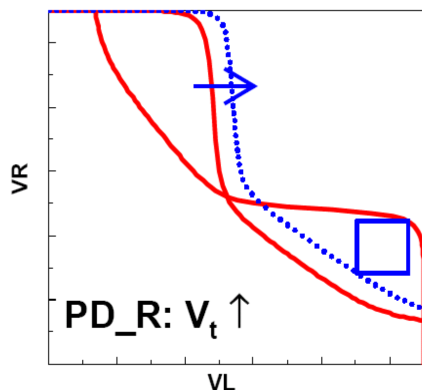
Effect of PBTI on SRAM

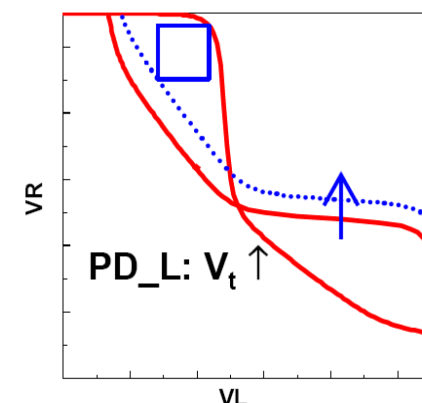




V_t increase in *one* nfet

– Worst case degradation, SNM decreases

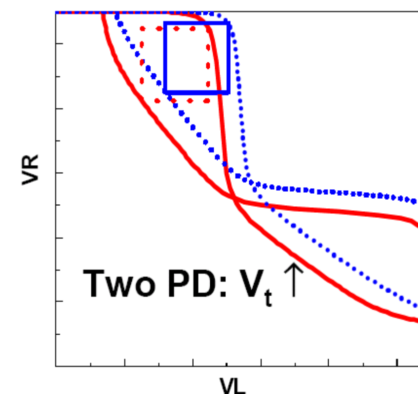




V_t increase in *both* nfets

– SNM better than asymmetric case

– Not worst-case



- J.C. Lin, *et al.*, IRPS 2007.

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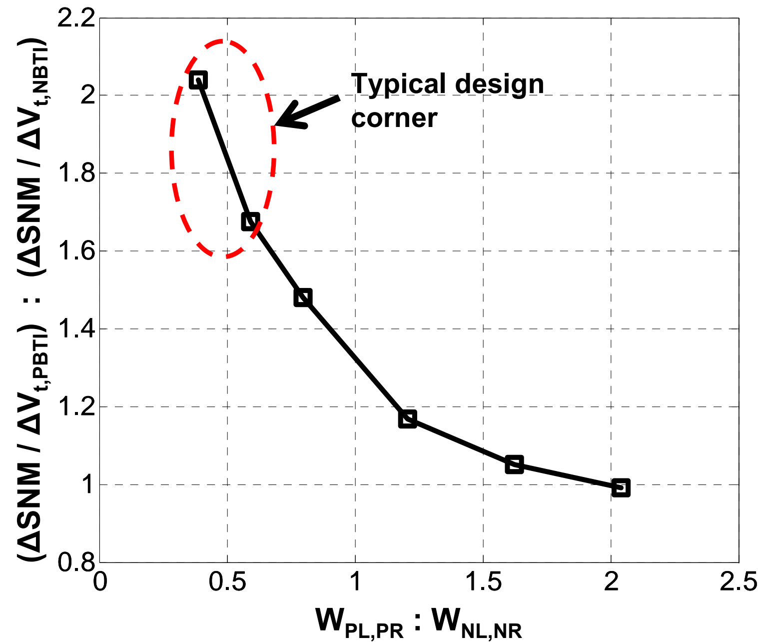
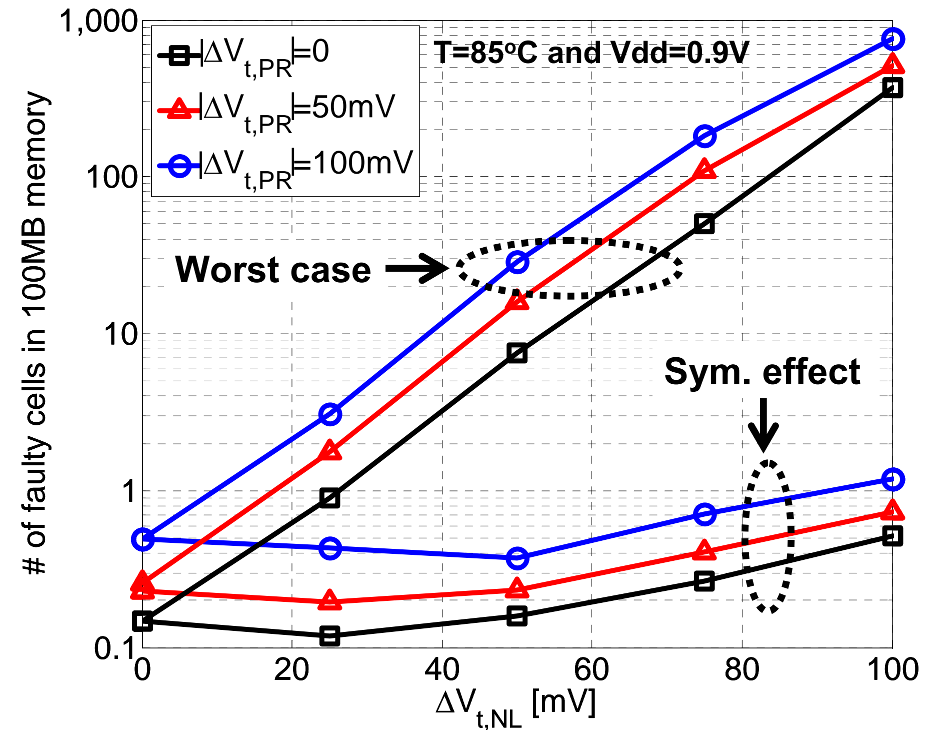
Effect of combined NBTI & PBTI

- **Relative sensitivity:**
  - SRAM cell is ~2x more sensitive to PBTI compared to NBTI



- **Symmetric degradation of cells leads to little increase in failure probability**
  - Worst case is asymmetric PBTI degradation



- A. Bansal *et al.*, IRPS 2009.

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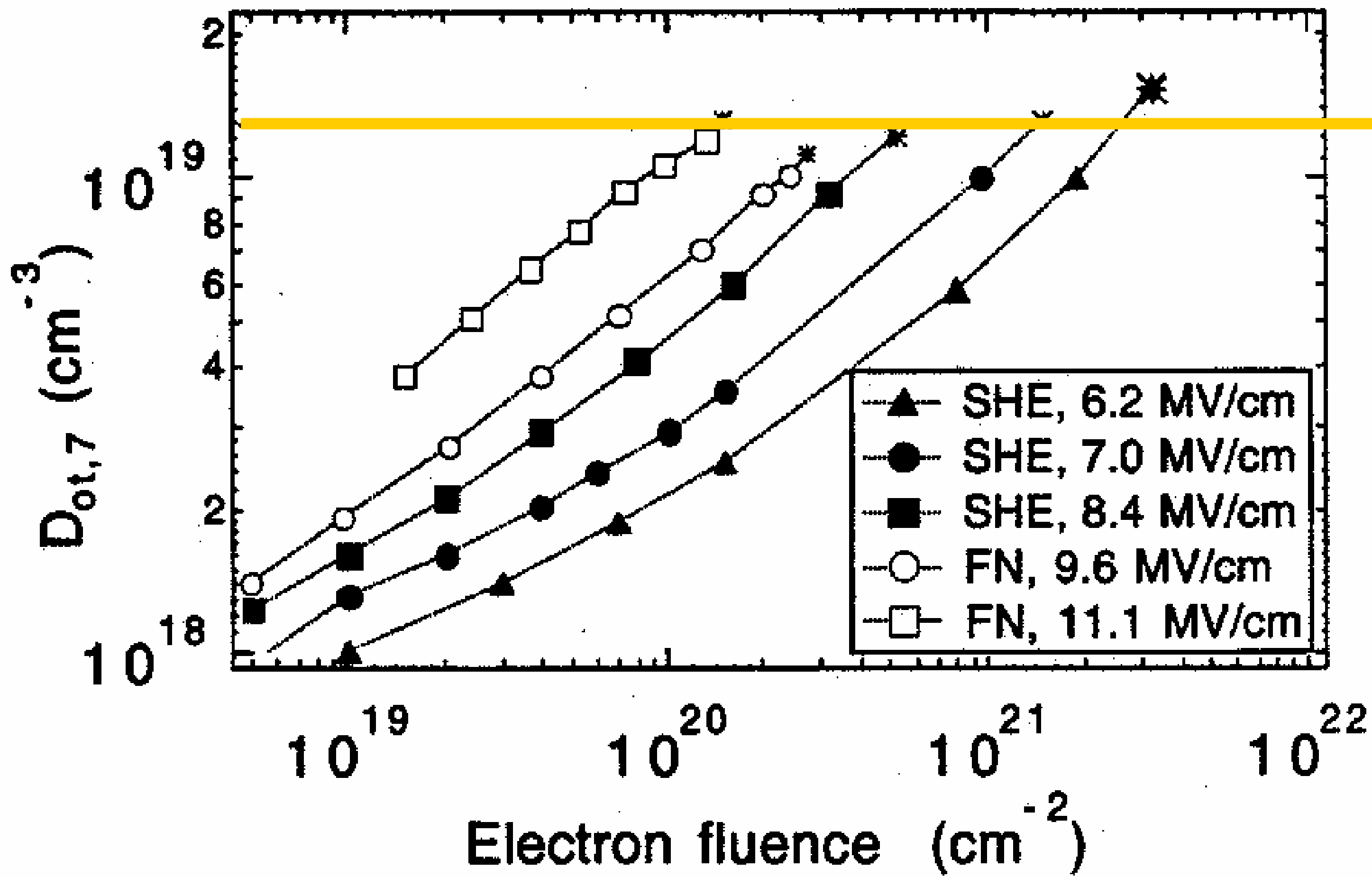
Oxide breakdown

- **Defect generation leading to breakdown**



Critical defect density **(N^{BD})**

- R. Degraeve *et al.*, TED **45**, 904 (1998).

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Statistical Distribution of Breakdown

- **Time-to-Breakdown (T_{BD}), or Charge-to-Breakdown (Q_{BD}), is a statistically distributed quantity**
  - Random defect generation
- **The Weibull Distribution is an 'extreme value' distribution in *ln(x)* and is appropriate for a "weakest-link" type of problem.**
  - The weakest link in a chain controls the failure of the whole chain
  - If any one spot on a dielectric breaks, the entire device is broken
  - If any transistor fails, the whole circuit or chip fails

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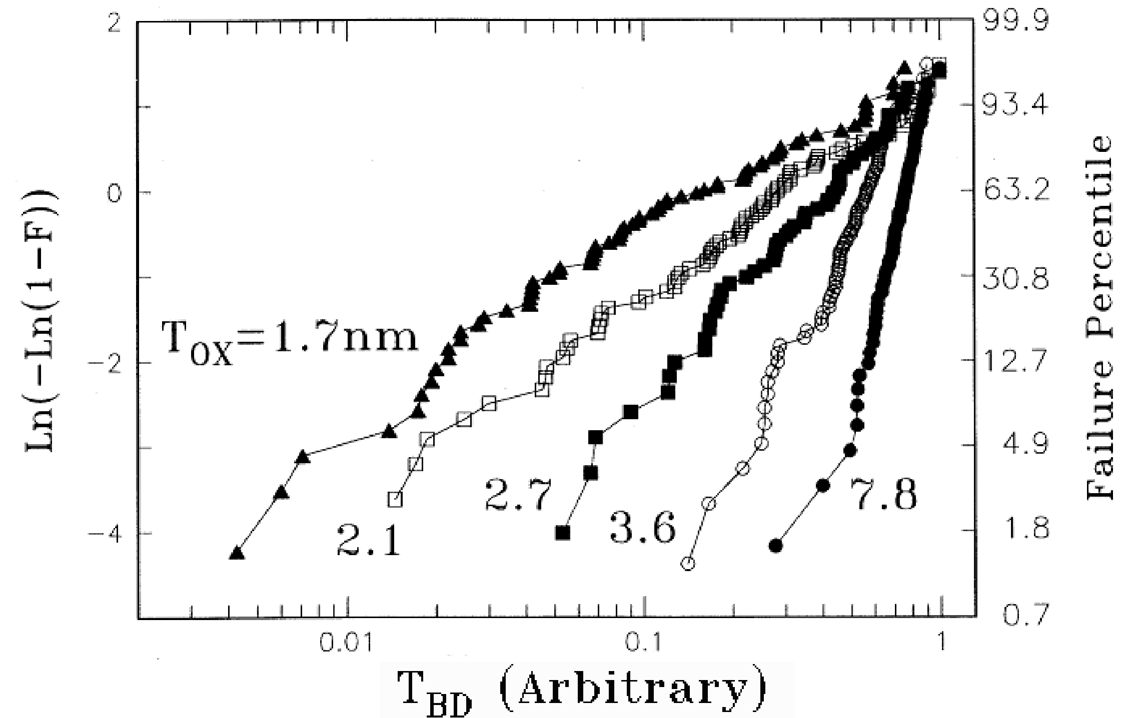
Weibull Distribution

$$F_{BD}(t) = 1 - e^{-\left(\frac{t}{T_{63}}\right)^{\beta}}$$

▪E.Y. Wu *et al*. Semic. Sci. Technol **15**, 425 (2000).



- *F* is the cumulative failure probability, i.e., the population fraction failed by age *x*, where *x* can be either charge or time.
- The characteristic life T_{63} corresponds to the charge or time where 63.2% of samples fail, and β is called the slope parameter, or Weibull slope.
- Plotting W≡*ln*[-*ln*(1-F)] against *ln*(*x*) gives a straight line with slope β.

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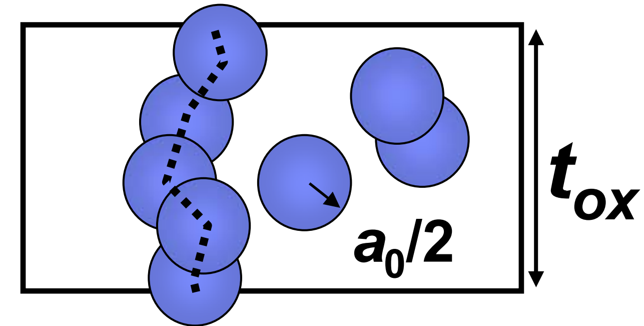
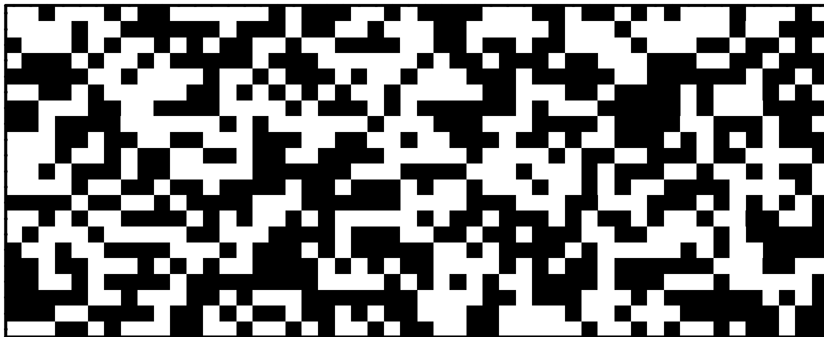
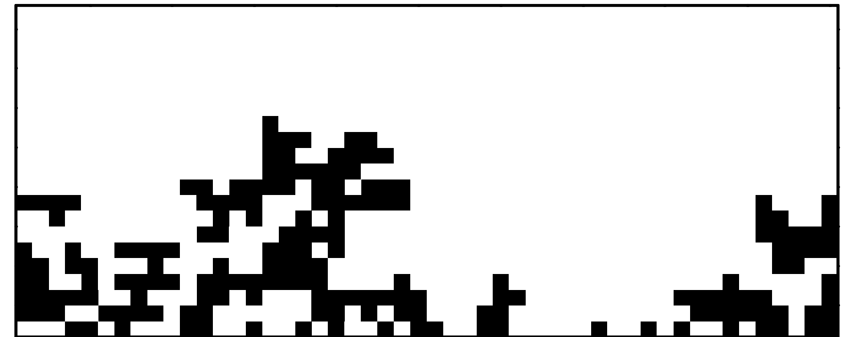
Thickness-dependent Weibull slope



- "Percolation" model
- **Defects generated randomly in oxide until a conducting ("percolating") path is formed**
  - Widely accepted, common to all physical models of defect generation
- **Explains thickness-dependent N^{BD} and Weibull slope**





- **Random defect generation**
- **Connection from one electrode toward the other**

- R. Degraeve *et al*., IEDM 1995, p. 866.
- J. H. Stathis, J. Appl. Phys. **86**, 5757 (1999).

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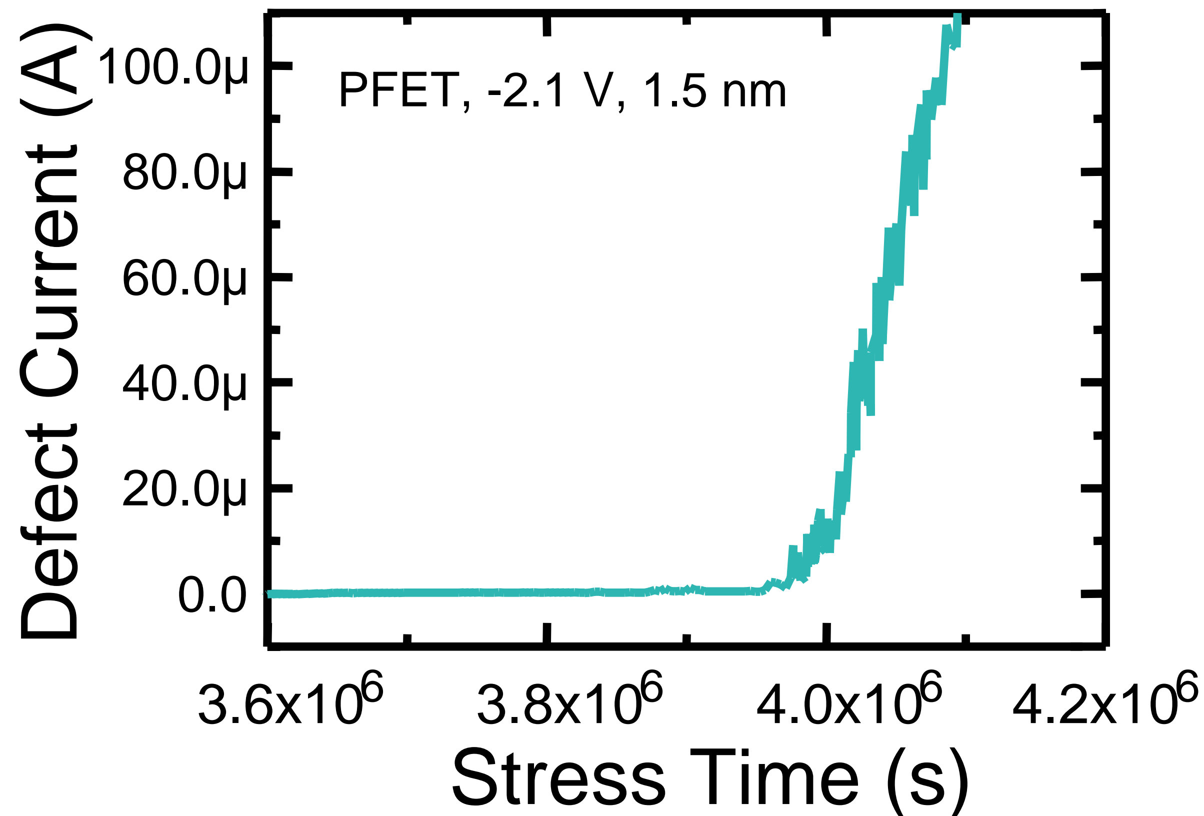
"Progressive" (gradual) breakdown

- **Gate breakdown is not a sudden, catastrophic process.**
- **It occurs gradually, over a measurable time scale.**



- F. Monsieur *et al.*, Microelectron. Reliab. **41**, 1035 (2001).
- B.P. Linder *et al.*, Electron Dev. Lett. vol 23, p. 661 (2002).
- T. Hosoi *et al.*, IEDM 2002, pp. 155-158
- F. Monsieur *et al.*, IRPS2002 and IRPS2003.
- B.P. Linder *et al.*, IRPS 2003, p. 402.

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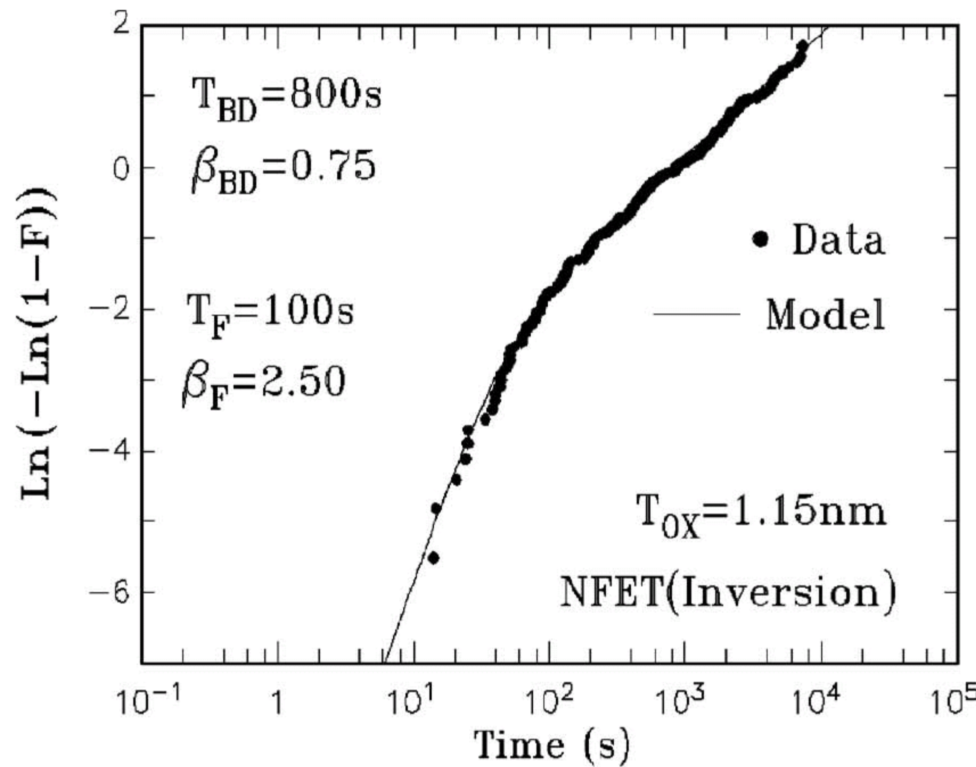
Weibull distribution plus progressive breakdown

$$f(t)=\int_0^\infty f_{BD}(t-\Delta t_{PBD})f_{PBD}(\Delta t_{PBD})d\Delta t_{PBD}$$



- Convolution of breakdown time distribution and post-breakdown growth time distribution
- Curvature on Weibull plot

$$F_{\mathrm{FAIL}}(t)=1-\exp\left\{-\left[\frac{\left(\frac{t}{T_F}\right)^{\beta_F}\left(\frac{t}{T_{\mathrm{BD}}}\right)^{\beta_{\mathrm{BD}}}}{\left(\frac{t}{T_F}\right)^{\beta_F}+\left(\frac{t}{T_{\mathrm{BD}}}\right)^{\beta_{\mathrm{BD}}}}\right]\right\}$$

- S. Tous *et al.*, Elec. Dev. Lett. 2008, p. 949.

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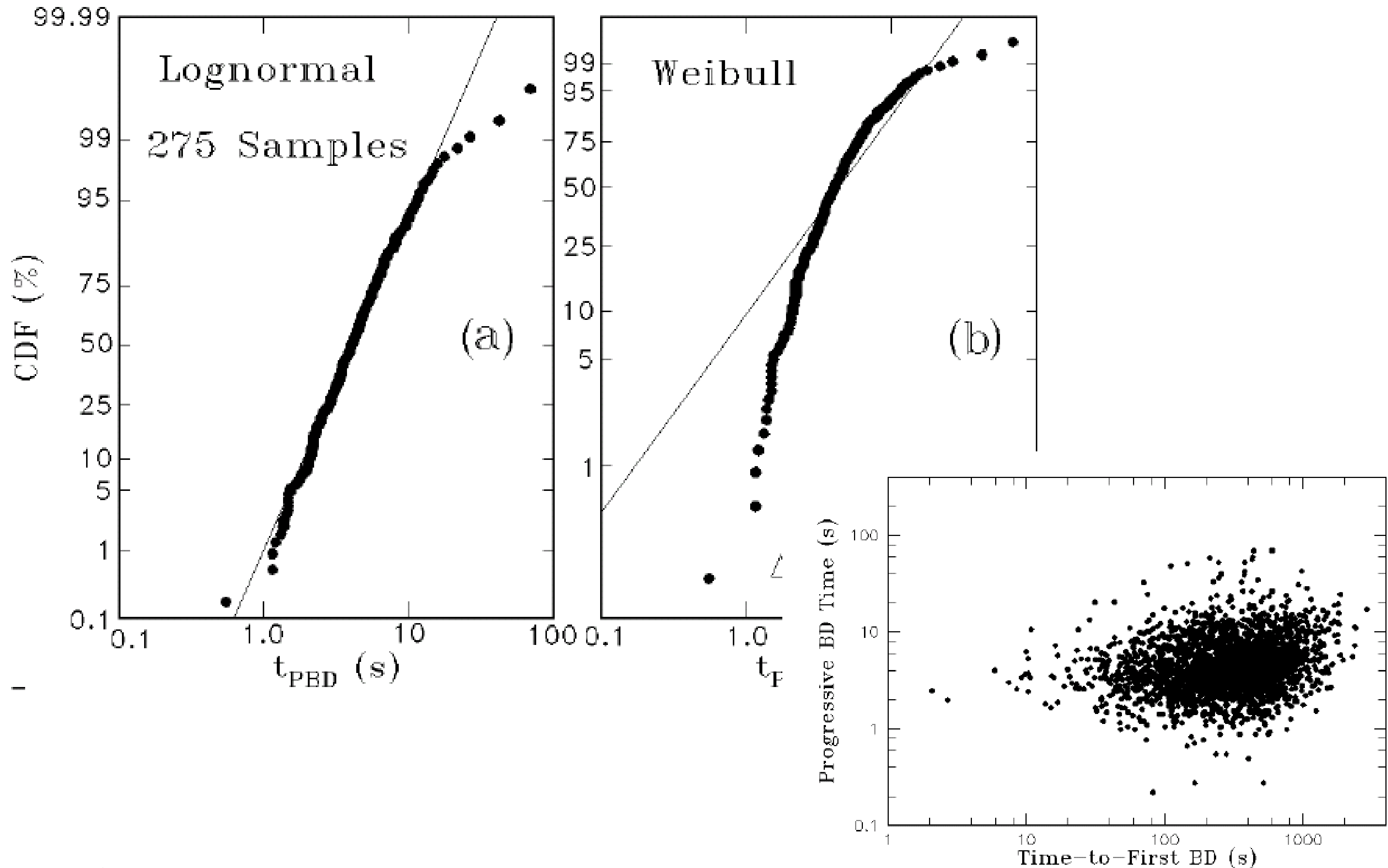
Post-breakdown growth time distribution



- E. Wu *et al.*, IEDM 2007, p. 493.

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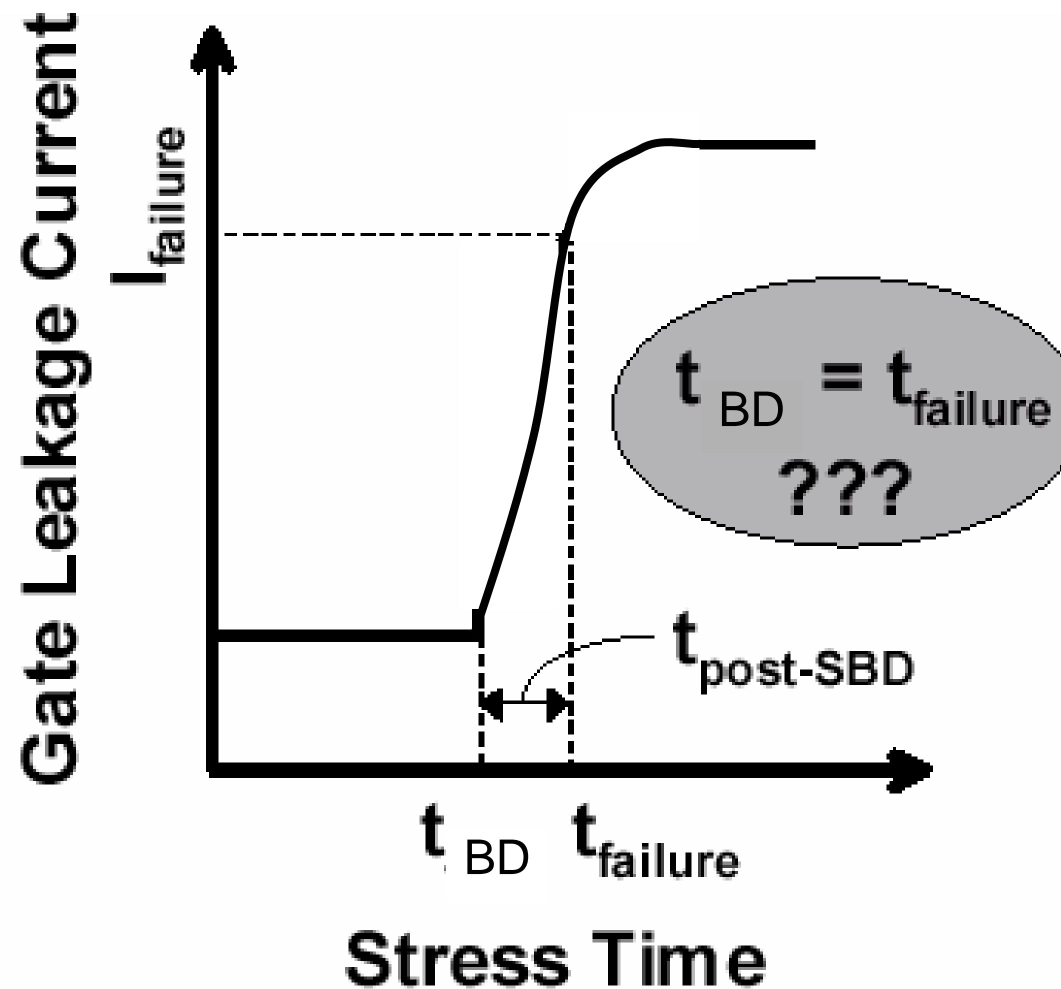
Progressive breakdown implications

➢ **When does a circuit fail?**



after T. Hosoi *et al*., SSDM 2002 pp. 155-158

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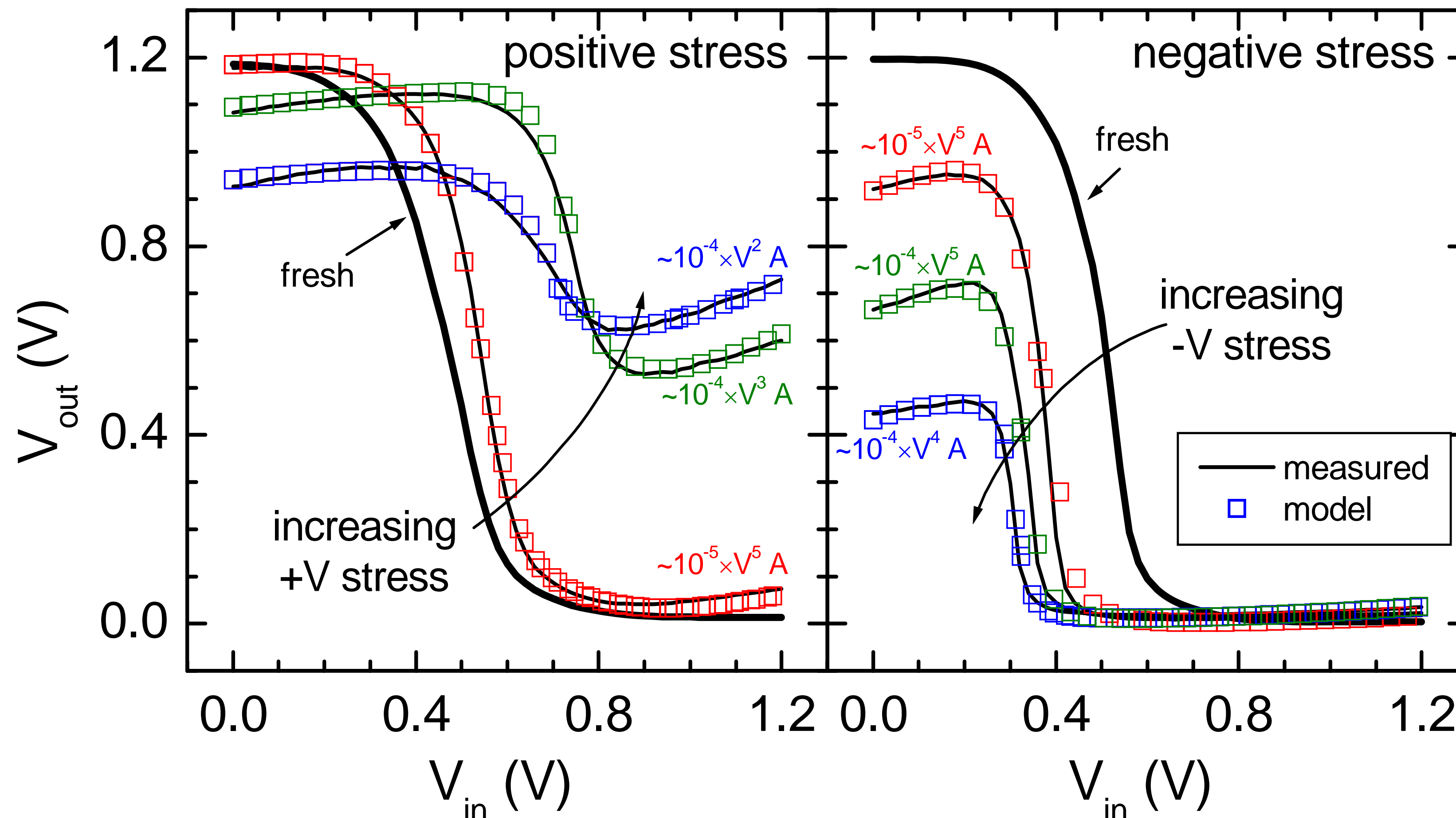
Transfer curves of inverters after oxide BD (experiment and model)



- R. Rodríguez *et al*.: IRPS 2003 p. 11; EDL **24**, 114 (2003); ESREF ’03.
- See further: B. Cheek *et al*.: IRPS 2004 p. 110.
  and: H-M. Huang et al., IRPS 2004 p. 593.

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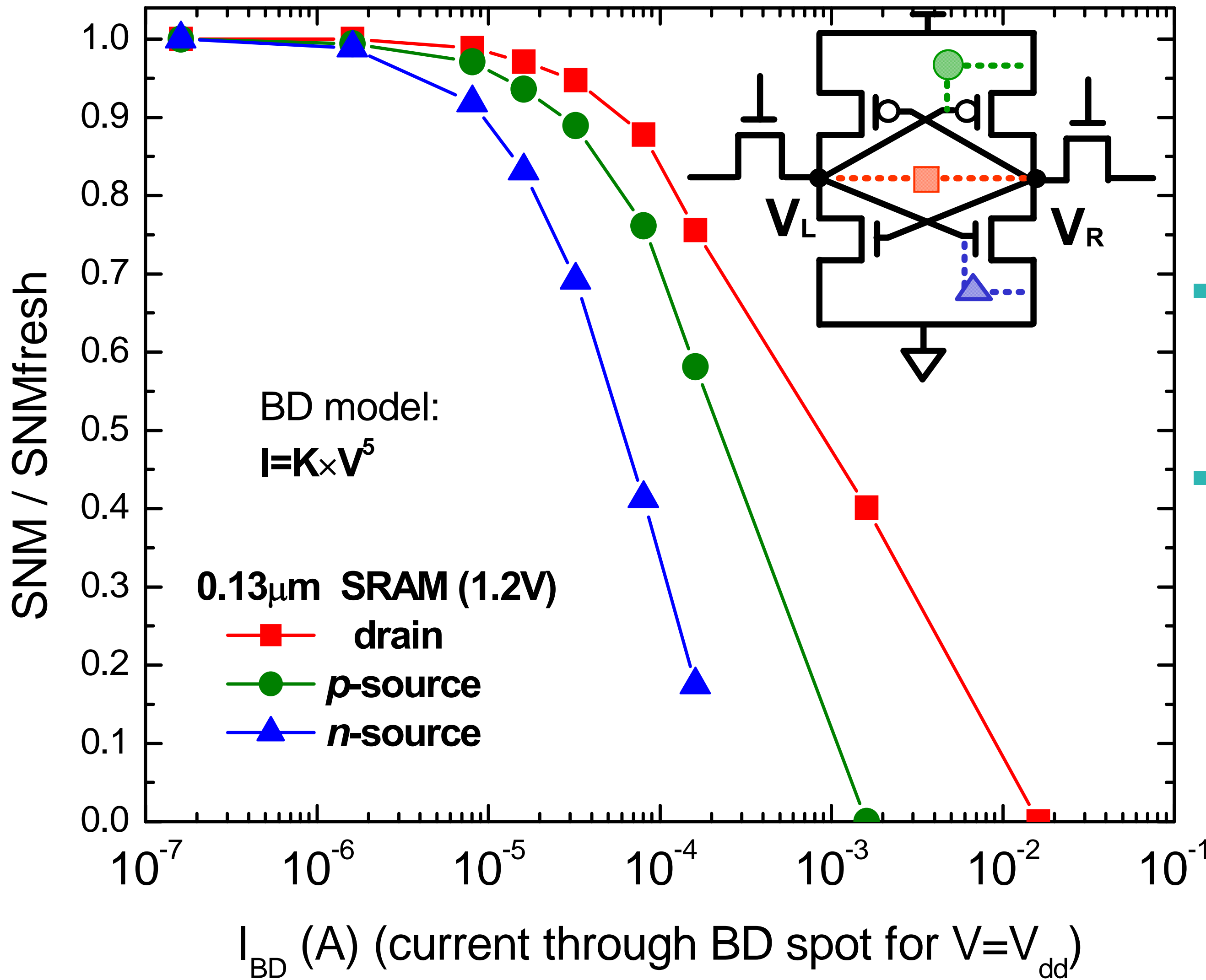
Effect of oxide breakdown on SRAM (model)



- **50% reduction in SNM for BD current > 50 µA**
- **worst case: *n*-source BD**
  - pulls down voltage at opposite node
  - loads weaker *p*-FET

▪ R. Rodríguez *et al.*, Electron Dev. Lett. **23**, 559 (2002).

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Summary: **effects of oxide wearout in circuits**

- **Negative Bias Temperature Instability (NBTI)**
- **Positive Bias Temperature Instability (PBTI)**
- **Hot Carrier Injection (HCI)**
  - All transistors in circuit may be degraded simultaneously, or particular individuals may be more vulnerable
    - Depending on circuit history

- **Oxide Breakdown (Progressive Breakdown)**
  - Generally, only one broken gate in a circuit
    - Breakdown is a statistically rare event

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Acknowledgements

- **Barry Linder**
- **Ernest Wu**
- **Aditya Bansal**
- **Sufi Zafar**
- **Andreas Kerber**
- **Ed Cartier**

  – This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

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