

# PPoPP 2008 Schedule

## WEDNESDAY

12:30 - 14:00 **Keynote (during lunch), Chair: Sid Chatterjee**

Compilers and Parallel Computing Systems  
*Frances Allen*

14:00 - 14:30 Break

14:30 - 14:35 Welcome

14:35 - 16:05 **Static analysis, Chair: Marc Shapiro**

Automatic Data Movement and Computation Mapping for Multi-level Parallel Architectures with Explicitly Managed Memories

*Muthu Baskaran, Uday Bondhugula, Sriram Krishnamoorthy, J Ramanujam, Atanas Rountev and P Sadayappan*

Type Inference for Locality Analysis of Distributed Data Structures

*Satish Chandra, Vijay Saraswat, Vivek Sarkar and Rastislav Bodik*

Quasi-Static Scheduling for Safe Futures

*Armand Navabi, Xiangyu Zhang and Suresh Jagannathan*

16:05 - 17:00 Break and poster set-up

17:00 - 19:00 **Poster session, with refreshments**

## THURSDAY

7:45 - 8:30 Continental breakfast

8:30 - 9:30 **Parallel algorithms, Chair: Greg Bronevetsky**

Scalable Packet Classification Using Interpreting -- A Cross-platform Multi-core Solution

*Haipeng Cheng, Zheng Chen, Bei Hua and Xinan Tang*

FastForward for Efficient Pipeline Parallelism: A Cache-Optimized Concurrent Lock-Free Queue

*John Giacomoni, Tipp Moseley and Manish Vachharajani*

9:30 - 10:30 **Matrix product for special platforms, Chair: Jeff Vetter**

Matrix Product on Heterogeneous Master-Worker Platforms

*Jack Dongarra, Jean-François Pineau, Yves Robert and Frédéric Vivien*

High Performance Linear Algebra on a Spatially Distributed Processor

*Jeff Diamond, Behnam Robatmili, Steve Keckler, Robert Van de Geijn, Kazushige Goto and Doug Burger*

10:30 - 11:00 Break

11:00 - 12:30 **GPUs and SIMD, Chair: Tim Harris**

Application Optimization and Performance Evaluation of a Multithreaded GPU Using CUDA

*Shane Ryoo, Christopher Rodrigues, Sara Bagsorkhi, Sam Stone, David Kirk and Wen- mei Hwu*

Massive Parallel LDPC Decoding on GPU

*Gabriel Falcão, Leonel Sousa and Vitor Silva*

A Case Study in SIMD Text Processing with Parallel Bit Streams

*Robert D. Cameron*

12:30 - 14:00 Lunch

14:00 - 15:00 **Programming model extensions, Chair: Lauren Smith**

Performance without Pain = Productivity: Data Layouts and Collectives in UPC

*Rajesh Nishtala, George Almasi and Calin Cascaval*

Programming with Tiles

*Jia Guo, Ganesh Bikshandi, Basilio Fraguera, Maria Garzaran and David Padua*

15:00 - 15:30 Break

15:30 - 17:30 **Runtime systems, Chair: Liviu Iftode**

SuperMatrix: A Multithreaded Runtime Scheduling System for Algorithms-by-Blocks

*Ernie Chan, Field G. Van Zee, Paolo Bientinesi, Enrique S. Quintana-Orti, Gregorio Quintana-Orti and Robert van de Geijn*

Design and Implementation of a High-Performance MPI for C# and the Common Language Infrastructure

*Douglas Gregor and Andrew Lumsdaine*

A Portable Runtime Interface For Multi-Level Memory Hierarchies

*Mike Houston, Ji-Young Park, Manman Ren, Timothy Knight, Kayvon Fatahalian, Alex Aiken, William Dally and Pat Hanrahan*

ZOID: I/O-Forwarding Infrastructure for Petascale Architectures

*Kamil Iskra, John W. Romein, Kazutomo Yoshii and Pete Beckman*

17:30 - 18:00 Break

18:00 - 19:30 Banquet

## FRIDAY

7:45 - 8:30 Continental breakfast

8:30 - 10:00 **Formal aspects of transactions and speculation, Chair: Philippas Tsigas**

Nested Parallelism in Transactional Memory

*Kunal Agrawal, Jeremy Fineman and Jim Sukha*

On the Correctness of Transactional Memory

*Rachid Guerraoui and Michal Kapalka*

Modeling Optimistic Concurrency via Quantitative Dependence Analysis

*Christoph von Praun, Rajesh Bordawekar and Calin Cascaval*

10:00 - 10:30 Break

10:30 - 12:30 **Panel: "Where Will All the Threads Come From?"**

Moderator: John Mellor-Crummey, Rice University

Panelists: John Feo (Microsoft), Sanjeev Kumar (Intel), Bradley Kuszmaul (MIT), Jan-Willem Maessen (Sun Microsystems), Keshav Pingali (University of Texas at Austin), Vivek Sarkar (Rice University)

12:30 - 14:00 Lunch

14:00 - 15:30 **Transactional memory I, Chair: Maged Michael**

Split Hardware Transaction: True Nesting of Transactions Using Best-effort Hardware Transactional Memory

*Yossi Lev and Jan-Willem Maessen*

Transactional Boosting: A Methodology for Highly-Concurrent Transactional Objects

*Maurice Herlihy and Eric Koskinen*

Concurrent GC Leveraging Transactional Memory

*Phil McGachey, Ali-Reza Adl-Tabatabai, Richard L. Hudson, Vijay Menon, Bratin Saha and Tatiana Shpeisman*

15:30 - 16:00 Break

16:00 - 17:30 **Transactional memory II: STM implementation, Chair: Bratin Saha**

Toward High Performance Nonblocking Software Transactional Memory

*Virendra Marathe and Mark Moir*

Dynamic Performance Tuning of Word-Based Software Transactional Memory

*Pascal Felber, Torvald Riegel and Christof Fetzer*

Software Transactional Memory for Large-Scale Clusters

*Robert Bocchino, Vikram Adve and Bradford Chamberlain*

17:30 - 17:45 **Best paper presentation and closing remarks**